IN THE CLAIMS:

1. A method of fabricating an integrated circuit, comprising the steps of:

forming a first interlevel dielectric over a semiconductor body;

forming a layer of resistor material over said first interlevel dielectric layer;

forming a metal stack on said layer of resistor material;

forming a first pattern over said metal stack;

etching said metal stack and said layer of resistor material using said first pattern;

removing said first pattern;

forming a second pattern to expose a portion of said metal stack over a thin film resistor area:

removing said exposed portion of said metal stack to form a thin film resistor.

- 2. The method of claim 1, wherein said second pattern is a photoresist pattern.
- 3. The method of claim 1, wherein said second pattern is a hardmask.
- 4. The method of claim 3, wherein said step of forming said second pattern comprises the steps of:

forming a hardmask layer over said metal stack;

forming a photoresist pattern over said hardmask layer to expose a portion of said hardmask layer over the thin film resistor area.;

removing said exposed portion of said hardmask layer; and removing said photoresist pattern.

5. The method of claim 4, wherein said hardmask layer comprises silicon dioxide.

- 6. The method of claim 1, wherein said interlevel dielectric layer comprises vias formed at a surface thereof.
- 7. The method of claim 1, wherein a portion of said metal stack remains at a first end and a second end of said thin film resistor.

8. A method of fabricating a thin film resistor in an integrated circuit, comprising the steps of:

providing a semiconductor body having a first interlevel dielectric layer; forming a layer of resistor material over said first interlevel dielectric layer; forming a metal stack on said layer of resistor material;

forming a first pattern over said metal stack, said first pattern covering said metal stack where a plurality of metal lines and said thin film resistor are desired;

dry etching said metal stack and said layer of resistor material using said first pattern to form said plurality of metal lines;

removing said first pattern;

forming a second pattern to expose a portion of said metal stack over a thin film resistor area;

removing said exposed portion of said metal stack using a wet etch to form said thin film resistor;

removing said second pattern; and

forming a second interlevel dielectric layer over said plurality of metal lines and said thin film resistor.

- 9. The method of claim 8, wherein said second pattern is a photoresist pattern.
- 10. The method of claim 8, wherein said second pattern is a hardmask.
- 11. The method of claim 10, wherein said step of forming said second pattern comprises the steps of:

forming a hardmask layer over said metal stack;

forming a photoresist pattern over said hardmask layer to expose a portion of said hardmask layer over the thin film resistor area.;

removing said exposed portion of said hardmask layer; and removing said photoresist pattern.

- 12. The method of claim 8, wherein said first interlevel dielectric layer comprises vias formed at a surface thereof.
- 13. The method of claim 8, wherein a portion of said metal stack remains at a first end and a second end of said thin film resistor.

- 14. An integrated circuit, comprising:
 - a first interlevel dielectric layer;
- a layer of resistor material located over a portion of said first interlevel dielectric layer;
- a plurality of metal interconnect lines located over a first portion but not a second portion of said layer of resistor material, wherein said second portion of said layer of resistor material forms a thin film resistor.
- 15. The integrated circuit of claim 14, further comprising a second interlevel dielectric layer over said thin film resistor and said plurality of metal interconnect lines.
- 16. The integrated circuit of claim 14, wherein a portion of said plurality of metal interconnect lines is electrically connected to an end portion of said thin film resistor.